#7 SP 7/1/02

PATENT APPLICATION
Do. No. 9898-176

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Dong-woo LEE and Ja-il KOO

Serial No. 09/898,699 Examiner: Not yet assigned

Filed: July 2, 2001 Group Art Unit: 2185

For: MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE

Date: December 14, 2001

Office of Petitions
Assistant Commissioner for Patents
Washington, D.C. 20231

APPLICANT'S REPLY TO DECISION

The Applicant is in receipt of a decision, dated November 5, 2001. The decision denies a Petition based on Applicant not submitting certain types of evidence. The decision invites the Applicant to submit it.

The Applicant resubmits the evidence herewith. It is a packet marked "Exhibit D".

[For the record, the Applicant mailed the same packet along with the Petition. From the verbiage of the Petition, however, it seems to not have been considered or received.]

The Applicant is now uncertain as to what the Petitions Office has received. Accordingly, the Applicant further submits Exhibit "E" in support of the petition (which is a substantial repetition of former Exhibit "C").

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Gregory T. Kavounas
Reg. No. 37,862

MARGER JOHNSON & McCOLLOM
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

COPY OF PAPERS ORIGINALLY FILED

Gp # 2185

PATENT APPLICATION
Do. No. 9898-176

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Dong-woo LEE and Ja-il KOO

Serial No. 09/898,699 Examiner: Not yet assigned

Filed: July 2, 2001 Group Art Unit: 2185

For: MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE

Date: December 17, 2001

Office of Petitions
Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL

Responsive to the Decision Refusing Status dated November 5, 2001, enclosed are the following:

[X] Applicant's Reply to Decision with Exhibits D and E.

[X] Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Gregory P. Kavounas
Reg. No. 37,862

MARGER JOHNSON & McCOLLOM
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Office of Petitions, Assistant Commissioner for Patents, Washington, DC 20231
Date: December 17, 2001
Marissa Thomas

COPY OF PAPERS ORIGINALLY FILED

O I P E JC73 JAN 2 2 2002 PATENT & TRADEMARK OFFICE

PTO/SB/17 (10-01)(modified)
OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

0002/PTO(modified) Rev. 10/2001

U.S. Department of Commerce
Patent and Trademark Office

FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT

Subtotal (1) + Subtotal (2) + Subtotal (3) = **($) 0.00**

Complete if Known	
Application Number	09/895,596
Filing Date	June 29, 2001
First Named Inventor	Rudolf H.J. Bloks
Group Art Unit	2183
Examiner Name	Not yet known
Attorney Docket Number	22300-05722

RECEIVED FEB 05 2002 Technology Center 2100

METHOD OF PAYMENT

1. The Commissioner is hereby authorized to:

☐ Charge the indicated fees to the below mentioned deposit account.

☒ Charge any additional fee required under 37 CFR 1.16 - 1.21 or credit any over payments to the below mentioned deposit account. †

☐ Applicant claims small entity status See 37 CFR 1.27

Deposit Account Number: 19-2555
Deposit Account Name: FENWICK & WEST LLP

A Duplicate Copy of this authorization is attached

2. ☐ **Payment Enclosed:**
☐ Check ☐ Credit Card ☐ Other

FEE CALCULATION (fees effective 10/01/2001)

1. FILING FEE

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description	Fee Due
101/$740	201/$370	Utility Filing	
106/$330	206/$165	Design Filing	
108/$740	208/$370	Reissue	
114/$160	214/$80	Provisional Filing	
		SUBTOTAL (1)	**($) 0.00**

2. CLAIMS

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description
103/$18	203/$9	Claims in excess of 20
102/$84	202/$42	Independent claims in excess of 3
104/$280	204/$140	Multiple dependent claim
109/$84	209/$42	Reissue independent claims over original patent
110/$18	210/$9	Reissue claims in excess of 20 and over original patent

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description	Fee Due
105/$130	205/$65	Surcharge - late filing fee or oath	
127/$50	227/$25	Surcharge-late provisional filing fee or cover sheet	
147/$2,520	147/$2,520	For filing a request for reexamination	
115/$110	215/$55	Extension for response within first month†	
116/$400	216/$200	Extension for response within second month†	
117/$920	217/$460	Extension for response within third month†	
118/$1,440	218/$720	Extension for response within fourth month†	
128/$1,960	228/$980	Extension for response within fifth month†	
119/$320	219/$160	Notice of Appeal	
141/$1,280	241/$640	Petition to revive unintentionally abandoned application	
142/$1,280	242/$640	Utility Issue Fee (Or Reissue)	
143/$460	243/$230	Design Issue Fee	
122/$130	122/$130	Petitions to the Commissioner	
126/$180	126/$180	Submission of Information Disclosure Statement	
179/$740	279/$370	Request for Continued Examination (RCE)	
581/$40	581/$40	Recording each patent assignment per property (times number of properties)	
146/$740	246/$370	Filing a submission after final rejection (37 CFR 1.129(a))	
149/$740	249/$370	For each additional invention to be examined (37 CFR 1.129(b))	
		Other fee *(specify)*:	
		Other fee *(specify)*:	
		SUBTOTAL (3)	**($) 0.00**

For	(Col. 1) No. of Existing Claims		(Col. 2) Highest No. Previously Paid For		(Col. 3) Extra**		Fee		Fee Due
TOTAL		minus*	20 or 0	=		x		=	
INDEP		minus*	3 or 0	=		x		=	
[ ] First presentation of multiple dependent claim								=	

* *Subtract the greater number of Col. 2*
** *If the difference between Col. 1 and Col. 2 is less than zero, then enter "0" in Col. 3*

SUBTOTAL (2) **($) 0.00**

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	Michael Plimier	Reg. Number	43,004
Signature		Date	December 10, 2001

22300/05722/DOCS/1229435.1

† *Request for Extension of Time per 37 CFR 1.136 (a)(3) made hereby*

COPY

PTO/SB/17 (10-01)(modified)
OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

0002/PTO(modified)
Rev. 10/2001

U.S. Department of Commerce
Patent and Trademark Office

FEE TRANSMITTAL

TOTAL AMOUNT OF PAYMENT

Subtotal (1) + Subtotal (2) + Subtotal (3) = **($) 0.00**

Complete if Known	
Application Number	09/895,596
Filing Date	June 29, 2001
First Named Inventor	Rudolf H.J. Bloks
Group Art Unit	2183
Examiner Name	Not yet known
Attorney Docket Number	22300-05722

RECEIVED
FEB 05 2002
Technology Center 2100

JAN 22 2002

METHOD OF PAYMENT

1. The Commissioner is hereby authorized to:

☐ Charge the indicated fees to the below mentioned deposit account.

☒ Charge any additional fee required under 37 CFR 1.16 - 1.21 or credit any over payments to the below mentioned deposit account. †

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Deposit Account Name: FENWICK & WEST LLP

A Duplicate Copy of this authorization is attached

2. ☐ **Payment Enclosed:**
☐ Check ☐ Credit Card ☐ Other

FEE CALCULATION (fees effective 10/01/2001)

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Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description	Fee Due
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106/$330	206/$165	Design Filing	
108/$740	208/$370	Reissue	
114/$160	214/$80	Provisional Filing	

SUBTOTAL (1) **($) 0.00**

2. CLAIMS

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description
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102/$84	202/$42	Independent claims in excess of 3
104/$280	204/$140	Multiple dependent claim
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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description	Fee Due
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127/$50	227/$25	Surcharge-late provisional filing fee or cover sheet	
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581/$40	581/$40	Recording each patent assignment per property (times number of properties)	
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149/$740	249/$370	For each additional invention to be examined (37 CFR 1.129(b))	
		Other fee *(specify)*:	
		Other fee *(specify)*:	

SUBTOTAL (3) **($) 0.00**

For	(Col. 1) No. of Existing Claims		(Col. 2) Highest No. Previously Paid For		(Col. 3) Extra**		Fee		Fee Due
TOTAL		minus*	20 or 0	=		x		=	
INDEP		minus*	3 or 0	=		x		=	
[ ] First presentation of multiple dependent claim								=	

* *Subtract the greater number of Col. 2*
** *If the difference between Col. 1 and Col. 2 is less than zero, then enter "0" in Col. 3*

SUBTOTAL (2) **($) 0.00**

SUBMITTED BY		Complete (if applicable)	
Typed or Printed Name	Michael Plimier	Reg. Number	43,004
Signature		Date	December 10, 2001

22300/05722/DOCS/1229435.1

† *Request for Extension of Time per 37 CFR 1.136 (a)(3) made hereby*

0001/PTO Rev. 10/95 U.S. Department of Commerce Patent and Trademark Office			
TRANSMITTAL FORM *(to be used for all correspondence during pendency of filed application)*		Application Number	**09/895,596**
		Filing Date	**June 29, 2001**
		First Named Inventor	**Rudolf H.J. Bloks**
		Group Art Unit Number	**2183**
		Examiner Name	**Not yet known**
Total Number of Pages in This Submission	**7***	Attorney Docket Number	**22300-05722**

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form (in duplicate)
  - ☐ Check Enclosed
- ☒ Return Receipt Postcard
- ☐ Response to Notice to File Missing Parts
- ☐ Assignment & Recordation Cover Sheet
- ☐ Declaration
- ☐ Power of Attorney
- ☐ Application Data Sheet
- ☒ Information Disclosure Statement & PTO-1449
  - ☒ Copies of IDS Cited References
- ☐ Request for Corrected Filing Receipt
- ☐ Request for Correction of Recorded Assignment
- ☐ Amendment/Response: [ ] Page(s)
  - ☐ After Final
- ☐ Status Request
- ☐ Revocation and Substitute Power of Attorney
- ☐ Issue Fee Transmittal
- ☐ Letter to Chief Draftsperson
- ☐ Formal Drawing(s):
  - [ ] Sheet(s) of Figure(s) [ ]
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Certified Copy of Priority Document(s)
- ☐ After Allowance Communication to Group
- ☐ _____
- ☐ _____
- ☐ _____
- ☐ _____
- ☐ _____
- ☐ _____

REMARKS: * Number of pages does not include cited references

SIGNATURE OF ATTORNEY OR AGENT

Signature:			
Attorney/Reg. No.:	**Michael Plimier, Reg. No. 43,004**	Dated:	**December 10, 2001**

CERTIFICATE OF MAILING

I hereby certify that this correspondence, including the enclosures identified above, is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on the date shown below. If the Express Mail Mailing Number is filled in below, then this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service pursuant to 37 CFR 1.10.

Signature:			
Typed or Printed Name:	**Michael Plimier**	Dated:	**December 10, 2001**
Express Mail Mailing Number *(optional)*:			

Representative Patent Attorney
YOUNG-PIL LEE *

Trademarks & Litigation
HOWARD JEAN [1][2]
HENG-SUP JIN [1]
HAK-DAE KIM [1]
JORDAN YONGSIK KIM *
NAM-JUNG HEO *
EUN-KYUNG AHN *
HEE-WON SEO *
JAE-HEUNG YOO

Biotechnology & Pharmaceutics
SUK-HEUM KWON *
SANG-BIN JEONG *
MOON-SUP LEE *
MIN-JEONG LIU *

JONG-CHEOL HYUN *
EUN-HEE JOO *

Chemistry & Material
KIL-SU KO *
TAE-HYONG KIM *
OHYEON HAHN
GIL-JA KWON
JUNG-SUN KIM
YI-JOO PARK
BO-HEE CHAI
BUM-TAK HAN
YOUNG-KI MIN

Mechanics
LEO LEE *
UN-SUK KOO *
JEONG-KEUN LEE *
HEUI-YOUNG JANG *
HYUN-TAE CHA *
JI-YOUNG SEO *

* Korean Patent Bar
[1] Korean Bar
[2] New York State Bar

Y.P. LEE & ASSOCIATES

PATENTS ◦ TRADEMARKS ◦ COPYRIGHTS

THE CHEONGHWA BUILDING
1571-18 SEOCHO-DONG, SEOCHO-GU
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Mechanics (Cont.)
HUN-CHUL PARK
MIN-HO CHO
SANG-JIN KIM
HYOUNG-SUK KO
CHANG-GIL JOO
SANG-TAE PARK
SANG-HYUN PARK
SU-KON EOU
GEUG-JAE JEONG
GONG-SOOK SOHN
MIN-HA JANG
SEONG-YONG LEE

Electronics
HEI-JEONG WON *
HEUNG-SOO CHOI *
HAE-YOUNG LEE *
YU-RI KIM *
JAE-SEOK YOON *
JAE-HO SHIN *
YEON-HEE KIM *

HO-KEUN LEE
BO-KYUNG PARK *
JAE-SEUNG YOON *
SO-HAK LEE *
CHAN-HONG JANG
SANG-HEE KIM
YOUNG-HO SHIN
KUY-HYUN KIM
WAN-HO KIM
JOONG-KEUN MOON
TAE-DONG KIM
SEOK-JIN HWANG
DAE-WOONG KIM
DONG-SUNG PARK
OH-JOON KWON
HYUN-JUNG KIM
WANG-PIL KIM
BUM-SIK PARK
IN-SUK LEE
JEE-HEE HAN
JAE-HOON SHIN
SEAN BAXENDELL
DAVID R. COOK
MAE YEE

19 July 2001

CONFIRMATION

Christina Borgens Lawton, Esq.
Marger, Johnson & McCollom, P.C.
1030 S.W. Morrison St.
Portland, Oregon 97205-2626
U.S.A.

VIA FAX & COURIER
(2 pages via fax)
Your Ref.: 9898-176
Our Ref.: SS-14849-US
S.E.C. Ref.: 00-37769
(Semiconductor Business)

Re: U.S. Patent Application corresponding to
Korean Patent Application No. 00-37769
Samsung Electronics Co., Ltd.

Dear Ms. Lawton:

This is further to our letter 29 June 2001 instruction you file the application without the Declaration and Assignment. Enclosed are materials proving that Mr. Ja-Il Koo, the non-signing inventor, could not be found in spite of Samsung's diligent efforts.

Eun-Joung Uhm, a member of Samsung In- House Patent Team, sent by certified mail and contents-certified mail a copy of the Specification, Claims, Declaration and Assignment to the last known address of the non-signing inventor, Mr. Ja-Il Koo, along with a letter requesting that he review the Application and sign and return the formal documents and Application. However, the formal documents were returned because Mr. Ja-Il Koo could not be found at that address.

Also, Eun-Joung Uhm sent an e-mail via "SINGLE", which is the internal network of Samsung, to Young-Woo Nam, a manager of the personnel Department in Samsung Electronics Co., Ltd., and Dong-Woo Lee, the joint inventor. However, in their replies to Eun-Joung Uhm's e-mail letter, both of the above people stated that Mr. Koo's whereabouts is unknown.

Also, Eun-Joung Uhm performed a Phone search on the Yahoo internet web site to try and locate Mr. Koo's whereabouts, but her efforts proved to be unsuccessful. Further, she searched for possible variations of the name "Ja-Il Koo" and contacted "Ja KOO" living in San

EXHIBIT D

in San Jose by phone because most employees who have stopped working for Samsung are known to live in San Jose. However Uhm's efforts have proved to be unsuccessful.

Although Samsung has tried to contact him to obtain his signature in many ways, their efforts have proved to be unsuccessful.

Please provide us with information as to how we should proceed as well as the necessary documents. We look forward to hearing from you soon

We appreciate your cooperation in this case.

Sincerely yours,

Y.P. LEE & ASSOCIATES

Jaseok Yoon

For the Firm

JSY/jas

Enclosures:

1. Copy of certified mail and contents-certified mail envelope to Mr. Koo and English translation thereof.(via courier only)

2. Copy of letter requesting that Mr. Koo review the Application and sign and return the formal documents and Application and English translation thereof.(via courier only)

3. Copy of e-mail letter sent to manager of personnel Department in Samsung Electronics Co., Ltd. and joint inventor and English translation thereof.(via courier only)

4. Copy of replies from manager of personnel Department in Samsung Electronics Co., Ltd. and joint inventor and English translation thereof.(via courier only)

5. Copy of results of phone search on Yahoo.(via courier only)

6. Copy of certification of working career Mr. Ja-Il Koo and English translation thereof.(via courier only)

[Material 1] 3 pages in total

From:

Samsung Electronics Co., Ltd.
Kyungki-do Yongin-city Kihung-eup Nongsuri San 24 bunji
Post Box: Suwon Post Office 37 ho
Tel: (Seoul) 760-7114 (info)
(Suwon) 209-7114 (info)
449-711
Samsung In-House Patent team, Eun-Joung Uhm

To:

Seoul Songpa-ku Karak-dong 176 bunji
Samhwan Apt 1-dong 1104-ho
Ja-Il Koo
138-745

Enclosures: English translated specification, Assignment, and Declaration

Mailing fee calculation

Amount: Original copy 24 pages
Sending means: special delivery mail fee (2,500)
2,500+11,500+1,100
=15,100 (Contents-certified mail fee)
2,500+900+140
=3,540 (certified Mail fee)
Total=18,640

Post Office Stamp

Returned on 27 June 2001 due to the recipient not living at the address
stamped by the mailman, Lee Soo Kil, an employee of the Seoul Song-pa Post Office.

[Material 2]

Sender:

Kyungki-do Yongin-city Kihung-eup San 24 bunji
Samsung Electronics Co., Ltd., Samsung In-House Patent Team
Eun-Joung Uhm

Recipient:

Seoul Songpa-ku Karak-dong 176 bunji
Samhwan Apt 1-dong 1104-ho
Ja-Il Koo

Enclosures: English translated specification, Assignment, and Declaration

Kyungki-do Yongin-city Kihung-eup San 24 bunji
Samsung Electronics Co., Ltd.
Representative director of board and Vice president
Jong-Yong Yoon (seal)

* If this letter is received by one other than the recipient, please return this letter to Samsung Electronics Co., Ltd.

It is certified that this mail was sent as a contents-certified mail on 26 June 2001 by the number 052266.

Postmaster of Shin-gal Post Office (stamp)

[Material 3]

To: Ja-Il Koo

Hello? Mr. Ja-Il Koo

I am Eun-Joung Uhm, a member of Samsung In-House Patent Team, We have tried to contact you many times but have not been successful. Thus, we inform you of the following.

Please return "English specification, Assignment and Declaration" sent on 25 June 2001 by 5 July.

"If we do not here [hear] from you to the contrary within two weeks of [from] the mailing date of this letter, we will interpret your sience [silence] as a refusal to sign the declaration or otherwise join in the application."

Then, we would like you to return the document as soon as possible. We wish you good luck.

25 June 2001

member of Samsung In-House Patent Team
Eun-Joung Uhm (Signature)

2 pages - total

[Material 4]

No. 01GB-0051422

Certification of Working Career

Department: Product Planning Team
Position: Manager
Name: a-Il Koo
Citizenship Registration No.: 591212-1000911
Present address: Seoul Songpa-ku Karak-dong 176 bunji Samhwan Apt 1-dong 1104-ho
Working period: from 1 Sep. 1999 to 30 Sep. 2000 (one year and one month)
Place of submission: U. S. Patent and Trademark Office
Purpose: submission

The undersigned certifies the above facts.

21 June 2001

Kyungki-do Yongin-city Kihung-eup San 24 bunji
Samsung Electronics Co., Ltd.
Representative director of board and Vice president
Jong-Yong Yoon (seal)

confirmed by Yeon-Sung Kim (sign) Chief of the department and Assistant manager (contact no.: 031-209-4128)

Material 4

제 01GB-0051422 호

경 력 증 명 서

소 속	상품기획팀	직 책	담당부장
성 명	구자일	주민등록번호	591212 - 1000911
현주소	서울특별시 송파구 가락동 176 삼환apt 1동 1104호		
근무기간	1999 년 09 월 01 일 부터 2000 년 09 월 30 일 까지 (1 년 1 개월)		
제출처	특허청		
용 도	제출용		

상기 사실을 증명합니다.

2001 년 06 월 21 일

三星電子株式會社

代表理事
副會長 尹鍾龍

부서장 확인: 직책 과장 성명 김연성

(인사부서 연락처 031 209 4128)

* 부서장 확인 날인 및 연락처가 없는 것은 무효입니다.

[Material 5]

Re: Inventor's signature

Created by Eun-Joung Uhm G1(a member of the Samsung Electronics Co., Ltd.)/application group (semiconductor)/Samsung Electronics Co., Ltd(June-26 2001 10:07:53)

Printed by Eun-Joung Uhm G1(a member of the Samsung Electronics Co., Ltd.)/application group (semiconductor)/Samsung Electronics Co., Ltd(June-26 2001 10:10:21)

Hello? I am Eun-Joung Uhm of Samsung In-House Patent Team.
I am looking for a contact point of a retired inventor to obtain a signature needed for filing an application in the U.S. If you know the contact point of Mr Ja-Il Koo who was a member of your department an quit the company on the end of September last year, please let me know. (Please reply by SINGLE.)

* Please reply if you do not know it.

Recipients:
manager of the personnel Department Samsung Electronics Co., Ltd.: Young- Woo Nam
Inventor's department: Dong-Woo Lee

[Material 6]

Re: Reply to the inventor's signature

Created by Young-Woo Nam G4(deputy)/ the department of personnel(Memory)/Samsung Electronics Co., Ltd (June-26 2001 10:46:33)
Printed by Eun-Joung Uhm G1(a member of the Samsung Electronics Co., Ltd.)/application group (semiconductor)/Samsung Electronics Co., Ltd(June-26 2001 10:46:51)

The only thing I know is the number of his mobile phone I gave you last time.

(Tel: 011-9116-267 tried on 4 July many times but not contacted) Eun-Joung Uhm (sign)

[Material 6]

Re: Reply to inventor's signature

Created by Dong-Woo Lee E5 (joint inventor) / Product Planning Team / Samsung Electronics Co., Ltd. (June-27 2001 09:17:13)
Printed by Eun-Joung Uhm G1(a member of the Samsung) / application group (semiconductor) / Samsung Electronics Co., Ltd.(June-27 2001 09:17:13)

I've heard that he is now in the U.S. But I do not have details in this regard.

발명자 싸인관련 Material 5

작 성 자 : 엄은정 G1(사원)/출원그룹(반도체)/삼성전자(2001-06-26 10:07:53)
인 쇄 자 : 엄은정 G1(사원)/출원그룹(반도체)/삼성전자(2001-06-26 10:10:21) UHM EUN JOUNG

안녕하세요? 지적자산팀 엄은정입니다.
미국출원시 필요한 발명자 싸인을 받기위해 퇴직한 발명자의 연락처를 찾고 있습니다.
퇴직 당시 조 과장님의 부서원이 었고 지난해 9월말에 퇴사한 "구자일" 씨의 연락처를 알고계시면
알려 주시면 고맙겠습니다.(SINGLE로 다시한번 보내주시면 감사하겠습니다.)

* 모르실경우라도 답장주시기 바랍니다.

수신인:
인사담당/ 남영우 대리님
발명자 부서/ 이동우 책임님

(답장) 발명자 싸인관련 Material 6

작 성 자 : 남영우 G4(대리)/인사그룹(MEMORY)/삼성전자(2001-06-26 10:46:33)
인 쇄 자 : 엄은정 G1(사원)/출원그룹(반도체)/삼성전자(2001-06-26 10:46:51)

제가 알고 있는것은 지난번에 통보드린 핸드폰번호 밖에 없습니다. T. 011-9116-2267.

전화시간 : 7/4/01
전화 : contact 이 안됨

UHM EUN JOUNG

-1-

(답장) (재전송) 발명자 싸인관련 Material 7

UHM EUN JOUNG

작 성 자 : 이동우 E5(책임)/상품기획팀/삼성전자(2001-06-27 09:16:35)
인 쇄 자 : 엄은정 G1(사원)/출원그룹(반도체)/삼성전자(2001-06-27 09:17:13)

현재 미국에 있는 것으로 알고 있고 자세한 것은 모릅니다.

이동우

Attorney's Docket No. 9898-176

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of: Dong-woo LEE and Ja-Il KOO

Serial No. 09/898,699 Examiner: Not Assigned

Filed: July 2, 2001 Group Art Unit: 2816

For: MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE

Office of Petitions
Assistant Commissioner for Patents
Washington, D.C. 20231

AFFIDAVIT

IN SUPPORT OF

PETITION MADE UNDER 37 C.F.R. §1.47(b)

By my signature at the end of this document, I hereby affirm the following:

1. My name is Gregory T. Kavounas; I am a patent attorney registered to practice in front of the United States Patent and Trademark Office ("PTO"); my PTO registration number is 37, 862; I work for the law firm of Marger, Johnson and McCollom ("MJM").

2. I and other attorneys from MJM are authorized to act in front of the PTO for patent matters on behalf of Samsung Electronics Co. ("Samsung"), a Korean company.

3. On July 2, 2001, one of the authorized attorneys of my law firm filed the above captioned patent application with the PTO on behalf of Samsung.

4. Samsung has a proprietary interest in the above captioned patent application. In particular, Samsung claims full ownership of all patent rights resulting from the patent application.

5. Samsung's claim of ownership is based on the fact that the patent application describes an invention made by two employees ("inventors") of Samsung, while in the employ of Samsung.

6. The two inventors are a) Mr. Dong-woo LEE and b) Mr. Ja-Il KOO.

7. The first one of the two inventors was available, and signed a Declaration Form, and an Assignment form. The last known address of this signing inventor is:

Mr. Dong-woo LEE
106-902, Huyndae Apt.,
Namsuwon, Annyung-ri,
Taean-eub, Hwasung-kun,
Kuyngi-do
Republic of Korea

8. The second one of the two inventors, namely Mr. Ja-Il KOO, has left the employ of Samsung, and can not be found. He has been unavailable for signing the Declaration Form. The last known address of this missing (nonsigning) inventor is:

Mr. Ja-Il Koo
1-1104, Samhwan Apt.,
Garak-dong, Songpa-gu,
Seoul,
Republic of Korea

9. A Korean patent law firm named Y.P. Lee & Associates ("Y.P. Lee") sometimes acts as intermediary between MJM and Samsung.

10. MJM has received from Y.P. Lee a packet ("Exhibit D") documenting Samsung's search for the missing inventor.

11. Exhibit D includes a cover letter (mailed July 19, 2001) to Ms. Christina Lawton of MJM. While not an attorney, Ms. Lawton is erroneously addressed as "Esq.".

12. The cover letter documents Samsung's search for the missing inventor, which is the remainder of the Exhibit D.

13. I believe Exhibit D to be genuine.

14. I believe that Samsung's search for the missing inventor has been more than diligent under the circumstances, as documented by Exhibit D.

15. Being hereby warned that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any resulting patent; I hereby declare and affirm that and all statements made of my own knowledge are true, and all statements made on information and belief are believed to be true.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Gregory T. Kavounas
Reg. No. 37,862

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

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Sorry, no people match the phone search criteria you entered.
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- Check for correct spelling in all search fields including City and State abbreviatic
- Broaden your search by using fewer search fields.
- Use the wildcard character ("*"). For example typing "D*" as your first name sea criteria will return people whose first names begin with "D".

It is also possible that the person you are looking for does not have a phone listing ir Yahoo! People Search.

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First: ja-il Last: koo

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State: Zip: Submit

searcher;

UHM EUN JOUNG.

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Name (click for details)	Address	Phone (click to call)	
Ja Koo	3808 S Bronson Ave Los Angeles , CA	(323) 295-6947	Want more informati Get a "US Search"
Ja Koo	200 S Olive St Los Angeles , CA	(213) 625-1207	Want more informati Get a "US Search"
Ja Koo	849 S Highland Ave Los Angeles , CA	(323) 857-1907	Want more informati Get a "US Search"
Ja Koo	6398 Lillian Way San Jose , CA	(408) 927-9748	Want more informati Get a "US Search"
Ja Koo	6554 Whitbourne Dr San Jose , CA	(408) 927-0437	Want more informati Get a "US Search"
Ja Koo	12221 Viewoak Dr Saratoga , CA	(408) 996-2200	Want more informati Get a "US Search"
Ja Koo	13230 Schoenborn St Sun Valley , CA	(818) 786-2071	Want more informati Get a "US Search"
Ja Koo	6711 Delco Ave Winnetka , CA	(818) 713-0400	Want more informati Get a "US Search"
Ja Koo	55 S Kukui St Honolulu , HI	(808) 529-0667	Want more informati Get a "US Search"
Ja Koo	744 Ekela Ave Honolulu , HI	(808) 732-2728	Want more informati Get a "US Search"

9/4/0 전화시도 → wrong person ↓ 당사의 퇴직자 대부분이 San Jose 지역에서 일하고 있으므로 연락 시도하였음

Most employees who have stopped working for Samsung are known to live in San Jose

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[Material 1]

25 pages ...

SAMSUNG

삼성전자

경기도 용인시 기흥읍 농서리 산24번지
사서함 : 수원우체국 37호
전 화 : (서울) 760-7114(안내)
(수원) 209-7114(안내)
449-711

지적재산팀 영문경

수량 : 원본 : 24장
발송수단 : 등기 (2,500)
⇒ 2,500 + 11,500 + 1100
= 15,100 ⇒ 내용증명
⇒ 2,500 + 900 + 140
= 3,540 (배달증명)
Total: 18,640

⇒ 잘 부탁드립니다.

우) 138-745

To. 서울특별시 송파구 가락동 176번지

삼환 Ⓐ 1동 1104호

구자일 님

반송

2001. 6. 27

배즘 ₩2980

※ 포함내용 : 명세서, Assignment, Declaration.

Material 2

보내는 사람: 경기도 용인시 기흥읍 산24번지
삼성전자반도체 지적자산팀
어 은 경

받는 사람: 서울특별시 송파구 가락동
176번지 사현상가 A 동 1104호
구 자 일 님

첨부내용: 양도명세서
Assignment
Declaration

京畿道 龍仁市 器興邑 農書理 山24番地
三星電子株式會社
代表理事 副會長 尹鍾龍

※ 본 서류를 다른 분이 받으셨다면
삼성반도체로 송부바랍니다.

이 우편물은 2001/06/26 제 052266
호에 의하여 내용증명우편물로
발송하였음을 증명함
신갈우체국장

Material 3

to. 국자일님

안녕하세요? 국자일님
삼성반도체 지적자산팀 염은경입니다.
여러차례 특허업무관련해서 연락을 시도하였으나,
연결이 되지않아 아래와 같이 통보드립니다.

이번 2001년 6월 25일자로 보내드리는
"영문명세서, Assignment, Declaration"을
7월 5일까지 회송하여 주시기 바랍니다.
"If we do not here from you to the contary within two weeks of the mailing date of this letter, we will interpret your sience as a refusal to sign the declartion or otherwise join in the application."
(7월 5일까지 회송되지 않으면, 선언서/양도증에
sign하는 것을 거부하는 것으로 간주하겠습니다.)

그럼, 기대하는 빠른 회송 바라오며, 항상 복운이
함께하시길 기원합니다.

2001년 6월 25일
삼성반도체 지적자산팀
사원. 염은경

이영필합동특허법률사무소
Y.P. LEE & ASSOCIATES
(137-874)서울시 서초구 서초동 1571-18 청화빌딩
TEL:(02)588-8585(代) FAX:(02)588-8586(代) E-mail:iplaw@yplee.co.kr http://www.yplee.co.kr

2001. 6. 8.
(☐ FAX ■ POUCH)

이특 제01H- 6861 호
발 신 : 삼성전자(주) 반도체 지적자산팀 출원그룹장 "관급회송"
담당자 : 지적자산팀으로
수 신 : 이동우, 구자일
제 목 : 미국 특허출원을 위한 2차 명세서 검토안 접수보고
[당소 참조번호: SS-14849-US]

1. 상기의 건에 대하여 미국 현지대리인으로부터 2차 명세서 검토안이 접수되어 당소의견과 함께 이를 보고 드리오니, 검토하신 후 선언서/양도증과 함께 **6월 20일**까지 귀사의 의견을 주시기 바랍니다.

2. 회송기한 : **6월 20일까지**

3. 미국 출원진행 사항

삼성 FILE 번호	IC200002-002US0	해외 발송일자	2000년 12월 02일
국내 출원번호	00-37769	국내 출원일자	2000년 7월 03일
특 허 명	정보의 비교-기록 기능을 구비하는 반도체 메모리 장치 및 이의 정보처리 방법		
발 명 자	이동우, 구자일		
해외 대리인	Mager Johnson McCollom		
중요, 일반 구분	☐ 중요특허 ■ 일반특허	특 허 등 급	A급
귀사검토의견	발명자 -	담당자	

2001. 01.6.22

4. 그 밖의 문의 사항은 반도체 특허그룹 해외출원담당 또는 특허사무소 해외 출원 담당으로 연락바랍니다.

특허사무소해외출원담당: 윤재석	TEL NO.	588-8585	FAX NO.	588-8547, 588-8548

* 첨부서류: 1. 현지대리인 서신 (01/06/05) 1부
2. 당소의견 1부
3. 명세서 검토안 1부
4. 선언서/양도증 1부

6.25 06

이영필합동특허법률사무소
대표변리사 이 영 필

1. 2001년 5월 29일의 이 동우씨와의 면담결과를 반영하여 청구항 제 11항 및 제 13항을 삭제하도록 지시하였습니다.

2. 미국 현지 대리인은 2001년 3월 31일자의 letter에서 제안한 것을 수용하여 미국 출원을 위한 최종 수정 명세서를 송부하여왔습니다.

그러나 page 7, line 19의 non-active는 **inactive**로 수정되어야 하며, Page 11, line 34의 .. through the second control pin은 **삭제**되어야 한다고 판단됩니다.

3. 그 밖의 청구항 및 명세서는 본원발명의 요지를 충분히 반영하고 있으므로, 현재의 수정명세서에서 page 7, line 19 및 Page 11, line 34를 수정하여 미국에 출원하는 것이 타당하다고 판단됩니다.

4. 첨부되는 ASSIGNMENT 및 COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION에 서명하신 후 **2001년 6월 20**일까지 상기 서류들을 당 사무소로 송부해 주십시오.

2001년 6월 8일 윤재석

PATENT APPLICATION
Attorney Docket No. 9898-176

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE, the specification of which is attached hereto:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Claiming Priority? Yes	No
00-37769	Republic of Korea	3 July 2000	☒	☐

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below: NONE

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application: NONE

I hereby appoint the following attorneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Attorney Name	Registration No.
Jerome S. Marger	26,480
Alexander C. Johnson, Jr.	29,396
Alan T. McCollom	28,881
James G. Stewart	32,496
Glenn C. Brown	34,555
Stephen S. Ford	35,139
Julie L. Reed	35,349
Gregory T. Kavounas	37,862
Scott A. Schaffer	38,610
Joseph S. Makuch	39,286
James E. Harris	40,013
Graciela G. Cowger	42,444
Ariel Rogson	43,054
Craig R. Rogers	43,888

Direct all telephone calls to Gregory T. Kavounas at (503) 222-3613 and send all correspondence to:

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, Oregon 97205

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Dong-woo LEE

Inventor's signature: _____ 01/06/12 (Date)

Residence: Kyungki-do, Republic of Korea

Citizenship: Republic of Korea

Post Office address: 106-902, Hyundae Apt., Namsuwon, Annyung-ri
Taean-eub, Hwasung-kun, Kyungki-do, Republic of Korea

Full name of second joint inventor: Ja-il KOO

Inventor's signature: _____ _____
(Date)

Residence: Seoul, Republic of Korea

Citizenship: Republic of Korea

Post Office address: 1-1104, Samhwan Apt, Garak-dong, Songpa-gu
Seoul, Republic of Korea

Subject: 9898-30: Revised Claims as allowed

Message:

PATENT APPLICATION
Atty's Do. No. 9898-176

ASSIGNMENT

U.S.A. Patent Application
Sole or Joint
For Inventions Made Outside U.S.A.
Executed With Application

In consideration of the sum of Ten Dollars (10.00) and other good and valuable considerations paid to each of the undersigned, to wit:

(1) **Dong-woo LEE**
(2) **Ja-il KOO**

☐ X if continued on separate page

the receipt and sufficiency of which are hereby acknowledged by the undersigned who hereby sell(s), assign(s) and transfer(s) unto:

SAMSUNG ELECTRONICS CO., LTD.
416 MAETAN-DONG, PALDAL-KU
SUWON-CITY, KYUNGKI-DO
REPUBLIC OF KOREA

(hereinafter designated "ASSIGNEE") the entire right, title and interest for the United States Of America as defined in 35 U.S.C. §1.00, in and to the invention known as:

MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE

for which an application for Letters Patent of the United States of America has been executed even date herewith by the undersigned, and in and to any and all divisionals, continuations, substitutes, and reissues thereof; and all resulting patents and the undersigned hereby authorizes and requests the United States Assistant Commissioner of Patents to issue said Letters Patent to the said ASSIGNEE, for its interest as ASSIGNEE, its successors, assigns and legal representatives; the undersigned agrees that the attorneys of record in said application shall hereafter act on behalf of said ASSIGNEE;

And the undersigned hereby agrees to testify and execute any papers for ASSIGNEE, its successors, assigns and legal representatives, deemed essential by ASSIGNEE to ASSIGNEE'S full protection and title in and to the invention hereby transferred.

Please sign
concurrently
with Oath or Declaration
and Power of Attorney

SIGNED ON THE DATES INDICATED BESIDE OUR SIGNATURES:

INVENTOR(S)	**DATE SIGNED**	**WITNESSED**
(1) Dongwoo Lee **Dong-woo LEE**	01/07/02	
(2) _____ **Ja-il KOO**		

FOR ADDITIONAL INVENTORS, "X" BOX ☐ AND CONTINUE ON SEC- 2.005

PLEASE RETURN RECORDED ASSIGNMENT TO:

Alan T. McCollom
Marger Johnson & McCollom
1030 S.W. Morrison Street
Portland, OR 97205

RGER JOHNSON & McCOLL

PROFESSIONAL CORPORATION

PATENT, TRADEMARK AND COPYRIGHT LAW,
TECHNOLOGY LICENSING & LITIGATION

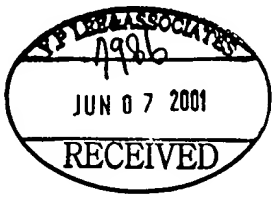
1030 S.W. MORRISON ST.
PORTLAND, OR USA
97205-2626
(503) 222-3613
FAX (503) 274-4622

Internet: christina@techlaw.com

June 5, 2001

VIA FACSIMILE
011-822-588-8586

Mr. Young-pil Lee
Y.P. Lee & Associates
The Cheonghwa Building
1571-18 Seocho-dong, Seocho-gu
Seoul, Rep. of Korea 137-073



Re: United States Patent Application
MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE
Korean Priority Document No.: 00-37769, filed July 3, 2000
Your Ref. No. SS-14849-US
Our Docket No.: 9898-176

Dear Mr. Lee:

Thank you for your facsimile of May 31, 2001. We have made your requested changes to the application and attach a revised draft to this fax. Additionally, we attach the required forms for the inventor's review and signature.

Please provide us your approval for filing this application, along with the executed forms, prior to the **July 3, 2001** filing deadline.

As always, please contact us if you have any questions.

Very truly yours,

MARGER JOHNSON & McCOLLOM, P.C.

/s/... Christina Borgens Lawton

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:clb

MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE

This application claims priority from Korean Priority Document No. 00-37769, filed on July 3, 2000 with the Korean Industrial Property Office, which document is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to memory devices, and more particularly, to memory devices having a Z-buffering function and method for depth compare-write used by the memory devices.

Description of the Related Art

In two-dimensional (2-D) graphics, an object on a display screen is represented by coordinates X, Y and color. When an existing object is replaced with a new object on a display screen, a color value is recorded at a position of a memory corresponding to coordinates X, Y of each pixel forming the new object, and then the color value is scanned on the display screen. By "object" it is meant a graphics object. The object may be called "new" from the graphics processing, even though it may be the same screen object perceived by the user.

In three-dimensional (3-D) graphics, Z-values represent a pixel's distance from the viewer. Typically, small Z values indicate that an object is close to the viewer, whereas large Z values indicate that the object is far away. In other words, Z-coordinate information determines depth data of an object on a display screen, thus allowing the user to recognize the depth of the object.

Devices that use 3-D graphics employ 3-D functions, which include Z-buffering, α-blending, and texture mapping. Such functions are computation intensive, and thus require a wide bandwidth. In particular, in Z-buffering, in order to perform 3-D graphic applications such as a 3-D game, Z-coordinate information should be added to X- and Y-coordinate information in a 2-D graphic. This serial operation is called Z-buffering.

In such functions, an existing object may be replaced by a new object on a display screen. It may be the same object, but with a new appearance, as would be mandated by the updated Z-coordinates.

Thus, when replacing an existing object with a new object on a display screen, firstly spatial coordinate values (also called Z values or depth data) of pixels are compared which map the existing object, against those which map the new object. Then, if the latter is less than the former, the former is updated with the latter.

Z-buffering is performed by comparing the Z-values of incoming color data with the Z-values of pre-existing color data. If the incoming color data is closer (i.e., it has a smaller Z value), the pre-existing color data is replaced with the incoming color data. Otherwise, the incoming color data is discarded.

In the prior art, this function is performed by the memory controllers. Such a memory controller reads the spatial coordinate values of the pixels of the existing object from a memory device, and compares them with the spatial coordinate values of the pixels of the new object. If there is any modification in the spatial coordinate values of the existing object, then the memory controller writes the spatial coordinate values of the new object to the memory device. This operation is called read-modify-write (hereinafter referred to as "RMW").

FIG. 1 is a timing diagram for explaining RMW of a conventional memory device. Referring to FIG. 1, if a memory read command RD is input on the rising edge of a clock cycle 3 after an activate command ACT is input from a memory controller, internal depth data Dout stored in a memory cell selected by the read command RD is read by the memory controller through data input/output (I/O) pins DQ.

The memory controller compares spatial coordinate values Dout of an existing object with input spatial coordinate values Din of a new object at intervals "a". As can be seen from Fig. 1, interval "a" is two cycles long. If the input spatial coordinate values (hereinafter referred to as "external depth data") Din of the new object are smaller than the spatial coordinate values (hereinafter referred to as "internal depth data") Dout of the existing object. It means that the object is now closer. The memory controller then prepares for writing the external depth data Din to a memory cell array of the memory device by replacing the internal data. If there is a write command WR, then the external depth data Din standing-by in the data I/O pins DQ is written to the selected memory cell array of the memory device, in response to the write command WR.

As can be seen in Fig. 1, for performing one RMW operation on spatial coordinate values, at least ten clock cycles are required from the point when the activate command ACT is input, until the point when a precharge command PRE may be input. This is because a

logic for comparing coordinate values of depth data is included in a memory controller, and a depth compare function is performed by the memory controller of the prior art.

Accordingly, the conventional memory device has a problem in that memory bus performance is degraded. The time taken for performing an RMW operation on spatial coordinate values is delayed, which degrades performance of the graphics functions.

SUMMARY OF THE INVENTION

To solve the above problems, it is a first objective of the present invention to provide a memory device which can shorten the time taken for modifying and writing spatial coordinate values, so as to improve the performance of a memory bus performing graphics.

It is a second objective to provide a method of processing depth data in a memory device for reducing the time needed to modify and write spatial coordinate values to improve graphics performance, as well as improving the performance of a memory bus.

Accordingly, to achieve the first objective, the present invention provides a memory device including a memory cell array, and a data modifying circuit for comparing external depth data of a new object received from the memory controller with internal depth data of an existing object. The internal depth data is stored in the memory cell array. The comparison is done between the data having representing coordinates of the new object and of the existing object. The internal depth data is replaced by the external depth data depending on the result of this comparison.

To achieve the second objective, the present invention provides a method of processing depth data of an object in a memory device controlled by a memory controller. The method includes the steps of: receiving external depth data of a new object from the memory controller, storing the received external depth data, comparing the stored external depth data with corresponding internal depth data stored in the memory device, and storing the external depth data with which the internal depth data is replaced depending on the result of the comparison in the step. A status signal may be outputted to the memory controller, indicating that the internal depth data has been modified.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objectives and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a timing diagram for explaining a read-modify-write (RMW) operation of a memory device in the prior art;

FIG. 2 illustrates a memory system including a memory device having a depth compare function according to an embodiment of the present invention;

FIG. 3 illustrates a detailed circuit for the memory device of FIG. 2;

FIG. 4 is a timing diagram illustrating a compare-read function according to an embodiment of the present invention; and

FIG. 5 is a flowchart for illustrating a method of comparing and reading depth data of an object in a memory device controlled by a memory controller according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 2, a memory system includes a memory device 22 according to the present invention, and is controlled by a memory controller 21. A monitor is not shown.

Furthermore, FIG. 2 shows a flow of a command signal CMD, which is generated by the memory controller 21, and is transmitted to the memory device 22. Other signals are also sent through control pins DC0 and DC1 and a data I/O pin DQ. The memory controller 21 also generates an address, which selects a specific memory cell of the memory device 22.

Furthermore, the memory controller 21 generates and transmits to memory device 22 a first control signal CS1 and a second control signal CS2 through the control pins DC0 and DC1, respectively. Control signals CS1 and CS2 may be active or non-active (implemented by choosing high and low levels). The memory controller 21also prepares for writing external depth data through the data I/O pin DQ.

The memory device 22 is controlled by the memory controller 21. The monitor displays an object having depth data modified by the memory device 22. The memory controller 21 provides an interface for performing various controlling tasks of the monitor and of the memory device 22.

The memory device 22 generates and sends to the memory controller 21 a first status signal SS1 and a second status signal SS2. If the first and second status signals SS1 and SS2 are in an active state (also called "HIT"), the memory controller 21 determines that internal depth data has been replaced by the external depth data. On the other hand, if the first and second status signals SS1 and SS2 are in an inactive state (also called "MISS"), the memory controller 21 determines that internal depth data is maintained.

In a preferred embodiment of the invention, the control signals CS1, CS2, travel through the same conductors as the status signals SS1, SS2, even though they travel in opposite directions. For example, status signal SS1 may be transmitted through first control pin DC0, and status signal SS2 may be transmitted through second control pin DC1.

This generates an advantageous economy in the construction of the invention. The economy is made possible by the fact that the control signals CS1, CS2, are generated and transmitted at different times than the status signals SS1, SS2, as will become clear from Fig. 4 later in this document.

Referring to FIG. 3, a detailed circuit of the memory device 22 of FIG. 2 is shown, which is made according to an embodiment of the present invention. The memory device 22 includes a data modifying circuit 30, a control circuit 31, a memory cell array 34, first and second control pins DC0 and DC1, and a data I/O pin DQ. In particular, the data modifying circuit 30 further includes a register 32 and a compare circuit 33.

The control circuit 31 receives external depth data of a new object through signal EDD being received from the data I/O pin DQ. Circuit 31 then outputs the external depth data EDD as either WTDC or NWT, in response to a first control signal CS1. If the first control signal CS1 is in a non-active state, the external depth data NWT is output to the memory cell array 34 for normal writing. This bypasses the remaining structure. On the other hand, if the first control signal CS1 is in an active state, the external depth data WTDC is output to the register 32 for depth compare writing.

The register 32 stores the output signal WTDC of the control circuit 31, i.e., the external depth data. The compare circuit 33 compares the data of the coordinates of a new object, which is output as RS from the register 32, with internal depth data Fcomp of the corresponding coordinates of an existing object, the internal depth data being stored in the memory cell array 34, in response to the second control signal CS2. If the output RS of the register 32, i.e., external depth data RS, is smaller than the internal depth data Fcomp, the compare circuit 33 outputs the external depth data RS to the memory cell array 34 in order to modify the internal depth data Fcomp. According to another embodiment of the invention, if the output RS of the register 32, i.e., external depth data RS, is larger than the internal depth data Fcomp, the compare circuit 33 outputs the external depth data comp to the memory cell array 34.

The compare circuit 33 outputs at least one status signal to the memory controller 21. If the internal depth data Fcomp is modified as a result of this comparison, the status signal is

a logic "high" signal HIT1 or HIT2. But if the internal depth data Fcomp is not modified, the status signal is a logic "low" signal MISS1 or MISS2.

FIG. 4 is a timing diagram when performing a compare-record function of the memory device 22 of FIG. 3 according to the present invention. A depth compare-write operation of the memory device 22 is now described in detail with reference to FIGS. 3 and 4. Referring to FIGS. 3 and 4, a depth compare-write command signal WR, first and second control signals CS1 CS2, and external depth data Dw, all of which are generated by the memory controller 21, are input into corresponding pins, i.e., a command pin (not shown), the first and second pins DC0 and DC1, and the data I/O pin DQ. This happens on the rise of the third cycle.

The control circuit 31 is now described. If the first control signal CS1 is in an active state when the write command signal WR is in an active state, the control circuit 31 outputs incoming external depth data WTDC to the register 32, in order to accomplish a depth compare-write function. Thus, the incoming external depth data EDD and the output signal WTDC of the control circuit 31 are the same. However, if the first control signal CS1 is in a non-active state, the control circuit 31 outputs the incoming external depth data NWT to the memory cell array 34 for writing.

Furthermore, if the first control signal CS1 is in an active state, the second control signal CS2 becomes important. In this case, the compare circuit 33 compares the internal depth data Fcomp within the memory cell array 34 with the output of the register 32, i.e., the external depth data RS.

Control signal CS2 becomes important as follows. If CS2 is in a non-active state, the compare circuit 33 compares the internal depth data Fcomp with the output of the register 32 in units of X bits, for example, 16 bits, where X is a natural number. But if the second control signal CS2 is in an active state, the comparison is in units of NX bits, for example, 32 bits if N is 2 and X is 16 where N and X are natural numbers.

As a result of comparing, the compare circuit 33 will write to the memory cell array 34 one of the two sets. In one embodiment it will be the set with the smallest depth values, and in another embodiment it will be the set with the largest depth values. This writing over the previous values has the effect of modifying the relevant stored values, if the different data has been overwritten.

The compare circuit 33 also issues status signals SS1, SS2, for reporting to the controller 21 whether the data has been changed or not. The status signals SS1, SS2 may be sent after only three (best case) or four (worst case) clock cycles lapse after issuing a depth

compare-write command (which was performed in cycle 3). Accordingly, the whole process may be completed on the 6th or 7th cycle, as opposed to the 10 cycles needed by the prior art.

If the compare circuit 33 compares in units of X bits, and if the data has been modified, the first status signal SS1 is a logic "high" signal HIT1, indicating that the lower X bits of the internal depth data Fcomp have been modified through the first control pin DC0. Furthermore, the second status signal SS2 is logic "high" signal HIT2, indicating that the upper X bits of the internal depth data Fcomp have been modified through the second control pin DC1.

If the compare circuit 33 compares in units of NX bits, and if the data has been modified, the first status signal SS1 is a logic "high" signal HIT1, indicating that lower NX bits of the internal Fcomp have been modified. But if the depth data has not been modified, the first and second status signals SS1, SS2 are logic "low" signals MISS1 and MISS2, indicating that the internal depth data Fcomp is maintained.

FIG. 5 is a flowchart showing a method of processing depth data of an object in the memory device 22 controlled by the memory controller 21, which starts from step 501. Referring also to FIGS. 2 and 3, in a step 503, the memory device 22 receives the external depth data EDD.

In step 505, the memory device 22 receives a first control signal CS1, and determines its state. If the first control signal CS1 is in a non-active state, then according to step 521, the control circuit 31 outputs the input external depth data EDD as data NWT to the memory cell array 34 within the memory device 22 for writing. But if the first control signal CS1 is in an active state, the control circuit 31 outputs external depth data EDD as data WTDC to the register 32.

In step 507, the memory device 22 receives a second control signal CS2, and determines its state. If the second control signal CS2 is in an active state, the compare circuit 33 compares the internal depth data Fcomp with the external depth data RS stored in the register 32 in units of NX bits (step 509). But if the second control signal CS2 is in an active state, the compare circuit 33 compares the internal depth data Fcomp with the external depth data RS in units of X bits (step 511).

In both instances, it is inquired whether the external depth data RS is smaller than the internal depth data Fcomp (step 513). If yes, the internal depth data Fcomp is modified to the external depth data RS (step 515). If not, the internal depth data Fcomp is maintained (step 517), and the external depth data RS is discarded. (In the equivalent embodiment, step 513 is

the opposite, inquiring instead whether the external depth data RS is larger than the internal depth data Fcomp.)

According to a next step 519, the result of the comparison is output to the controller, and the process ends (step 523). The result of the comparison is expressed via status signals SS1, SS2. These can acquire values as described above. Logic "high" and "low" values may equivalently be chosen.

As has been described in the foregoing, according to the conventional art, at least ten clock cycles are required for one read-modify-write ("RMW") operation. However, according to the present invention, only six (6) or seven (7) clock cycles are sufficient for performing one RMW operation, instead of the ten (10) required in the prior art . Therefore, the invention can improve performance by more than 30% compared with the prior art.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, the illustrated embodiments are only examples, and it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

What is claimed is:

1. A memory device for use with a memory controller, the memory device comprising:

a memory cell array adapted to store internal depth data of an object; and

a data modifying circuit distinct from the memory controller, the data modifying circuit being adapted to

receive corresponding new external depth data of the object from the memory controller,

compare the new external depth data with the internal depth data, and

write the external depth data in the memory cell array over the internal depth data depending on the result of the comparison.

2. The memory device of claim 1, wherein

the data modifying circuit is further adapted to output to the memory controller a status signal.

3. The memory device of claim 1, further comprising:

a first control pin for receiving a first control signal from the memory controller; and

a control circuit for transmitting the external depth data to the memory cell array thereby bypassing the data modifying circuit depending on a state of the first control signal.

4. The memory device of claim 3, wherein

the data modifying circuit is further adapted to output to the memory controller a status signal.

5. The memory device of claim 4, wherein

the status signal is output through the first control pin.

6. The memory device of claim 1, wherein the data modifying circuit includes

a register for storing the received new external depth data; and

a compare circuit for comparing the stored new external depth data with the internal depth data and for writing the external depth data in the memory cell array depending on the result of the comparison.

7. The memory device of claim 6, wherein

the compare circuit is further adapted to write the external depth data in the memory cell array if the external depth data is smaller than the internal depth data.

8. The memory device of claim 6, wherein

the compare circuit is further adapted to output a status signal to the memory controller.

9. The memory device of claim 6, further comprising:

a second control pin for receiving a second control signal from the memory controller,

wherein the compare circuit compares the internal depth data with the stored external depth data in units of X bits when the second control signal is in a non-active state, and in units of NX bits when the second control signal is in an active state.

10. The memory device of claim 9, wherein

if the second control pin is in an inactive state, the compare circuit outputs to the memory controller:

a first status signal indicating that the lower X bits of the internal depth data have been modified, and

a second status signal indicating that the upper X bits of the internal depth data have been modified.

11. The memory device of claim 9, wherein

if the second control pin is in a non-active state, the compare circuit outputs to the memory controller a status signal indicating that NX bits of the internal depth data have been modified.

12. A method of processing depth data of an object in a memory device controlled by a memory controller, the method comprising the steps of:

(a) receiving external depth data of the object from the memory controller;

(b) storing the received external depth data;

(c) receiving a first control signal from the memory controller through a first control pin distinct from the memory controller;

(d) determining a state of the first control signal; and

(e) if the state of the first control signal is determined to be inactive, writing the external depth data to a memory cell array within the memory device,

(f) elseif the state of the first control signal is determined to be active, comparing the stored external depth data with corresponding internal depth data stored in the memory cell array, and writing the external depth data over the corresponding internal depth data in the memory cell array depending on the result of the comparison.

13. The method of claim 12, wherein

step (f) further includes outputting to the memory controller a status signal indicating that the internal depth data has been modified.

14. The method of claim 12, wherein

writing in step (f) takes place if the comparison yields that the external depth data is smaller than the internal depth data.

15. The method of claim 12, wherein

writing in step (f) takes place if the comparison yields that the external depth data is larger than the internal depth data.

16. The method of claim 12, further comprising:

(g) receiving a second control signal from the memory controller through a second control pin distinct from the memory controller;

(h) determining a state of the second control signal; and

(i) if the state of the second control signal is determined to be inactive, comparing the internal depth data with the stored external depth data in units of X bits,

(j) elseif the state of the second control signal is determined to be active, comparing the internal depth data with the stored external depth data in units of NX bits.

17. The method of claim 16, wherein step (i) further includes

outputting to the memory controller a first status signal indicating that the lower X bits of the internal depth data have been modified, and

outputting to the memory controller a second status signal indicating that the upper X bits of the internal depth data have been modified ~~through the second control pin~~.

18. The method of claim 17, wherein

the first status signal is output through the first control pin, and

the second status signal is output through the second control pin.

19. The method of claim 16, wherein step (j) further includes

outputting to the memory controller a status signal indicating that the NX bits of the internal depth data has been modified.

20. The method of claim 19, wherein

the status signal is output through one of the first and second control pins.

ABSTRACT OF THE DISCLOSURE

A memory device for performing graphics functions, and a method of processing depth data that is received by a memory controller. The memory device includes a memory cell array, and a data modifying circuit. The data modifying circuit includes a register for storing external depth data received from the memory controller. The data modifying circuit also includes a compare circuit which compares the stored external depth data with corresponding internal depth data stored in the memory cell array, and updates the memory cell array accordingly. The compare circuit also outputs status signals, thus reporting to the memory controller whether the data was updated or not. Depending on a first control signal, a control circuit helps the external data be written directly to the memory, bypassing the data modifying circuit. Depending on a second control signal, the comparison is in X bits or NX bits.